杭芯科技
HUTCHIP

HC3139KT

20V P-Channel MOSFET

General Description

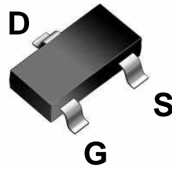
These P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

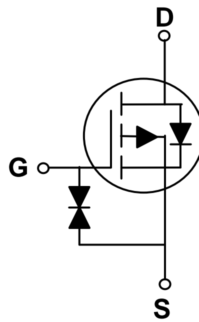
Features

V_{DS}	-20V
I_D (at V_{GS}=-4.5V)	-0.5A
$R_{DS(ON)}$ (at V_{GS}=-4.5V)	580mΩ(Typ)

ESD Protected Up to 2.0KV (HBM)

SOT723





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	±12	V
Drain Current-Continuous	TC=25°C	I_D	-0.5	A
	TC=100°C	I_D	-0.4	A
Maximum Power Dissipation		P_D	0.18	W
Drain Current – Pulsed1		I_{DM}	-2.6	A
Junction and Storage Temperature Range		T_J,T_{STG}	-55 To 150	℃

Thermal Characteristics

Parameter	Symbol	Typ	Max	Unit
Thermal Resistance junction-to-solder point	$R_{\theta Jsp}$		40	℃ /W
Thermal Resistance junction-to-Ambient	$R_{\theta JA}$		500	℃ /W

Electrical Characteristics (TJ=25℃ unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V I_D=-250μA	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-20V,V_{GS}=0V			1	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±10V,V_{DS}=0V			±10	μA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=-250μA	-0.3		-1.2	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=-4.5V, I_D=-0.5A		580	850	mΩ
		V_{GS}=-2.5V, I_D=-0.3A		850	1200	mΩ
		V_{GS}=-1.8V, I_D=-0.2A		1350	2000	mΩ
I_S	Maximum Body-Diode Continuous Current				-0.5	A
DYNAMIC PARAMETERS						
Ciss	Input Capacitance	V_{DS}=-10V,V_{GS}=0V, F=1.0MHz		71		pF
C_{oss}	Output Capacitance			20		pF
C_{rss}	Reverse Transfer Capacitance			15		pF
SWITCHING PARAMETERS						
$t_{d(on)}$	Turn-on Delay Time	V_{DD}=-10V,I_D=-0.2A, V_{GS}=-4.5V, R_G=10Ω		4		nS
t_r	Turn-on Rise Time			19		nS
$t_{d(off)}$	Turn-Off Delay Time			16		nS
t_f	Turn-Off Fall Time			25		nS
Q_g	Total Gate Charge	V_{DS}=-10V,I_D=-0.2A, V_{GS}=-4.5V		1.2		nC
Q_{gs}	Gate-Source Charge			0.37		nC
Q_{gd}	Gate-Drain Charge			0.27		nC
V_{SD}	Diode Forward Voltage	V_{GS}=0V,I_{SD}=-1A		0.7	1.2	V

Note：

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%.
3. Essentially independent of operating temperature.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

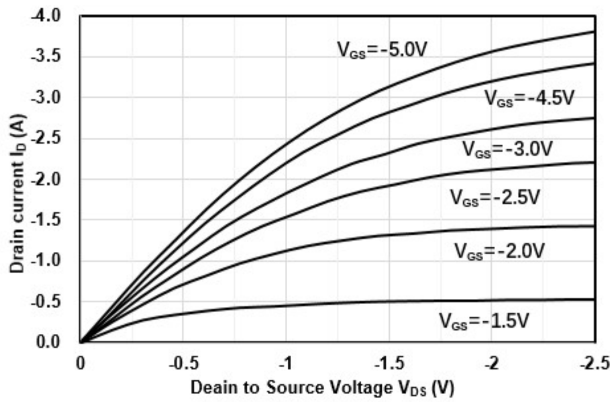


Figure1. Output Characteristics

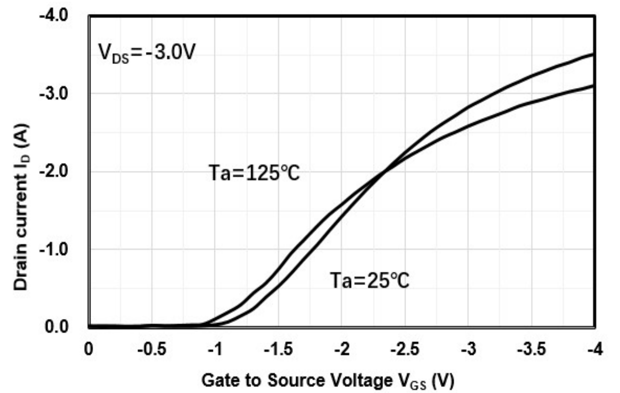


Figure2. Transfer Characteristics

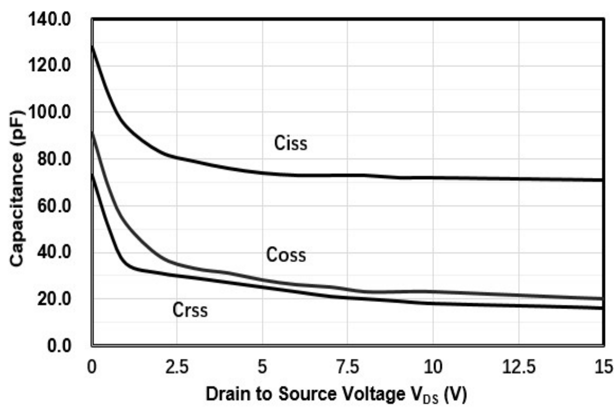


Figure3. Capacitance Characteristics

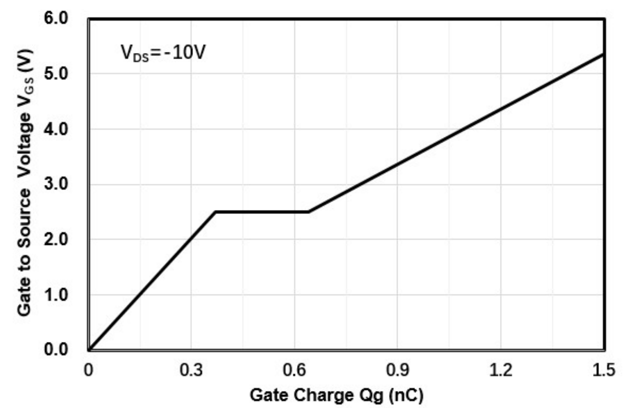


Figure4. Gate Charge

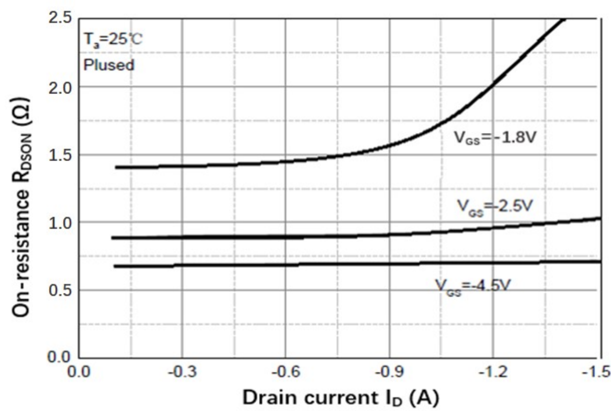


Figure5. Drain-Source on Resistance

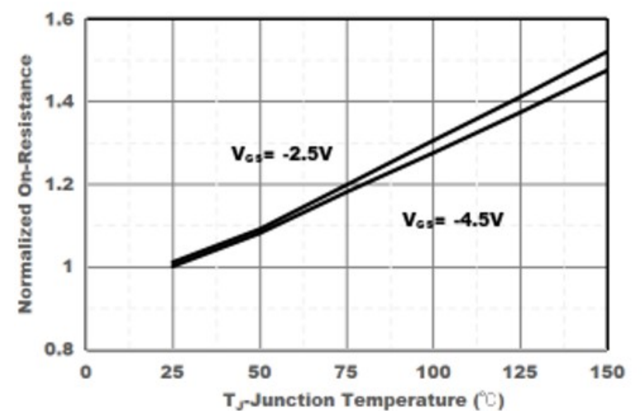


Figure6. Drain-Source on Resistance

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

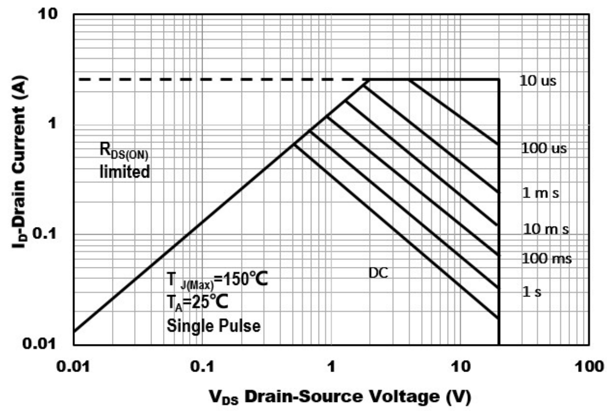


Figure7. Safe Operation Area

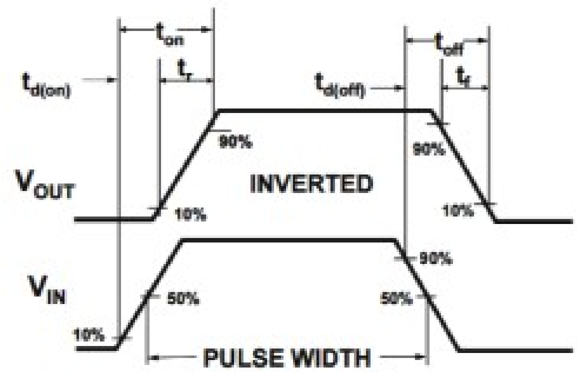
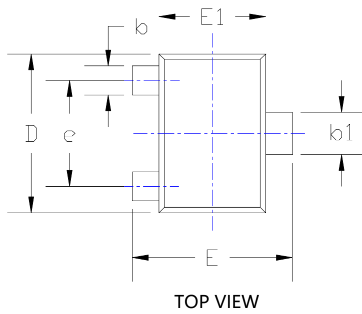
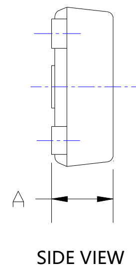


Figure8. Switching wave

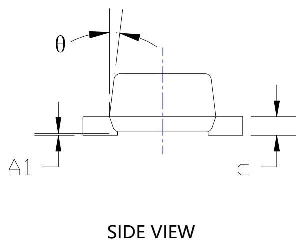
SOT723 PACKAGE INFORMATION



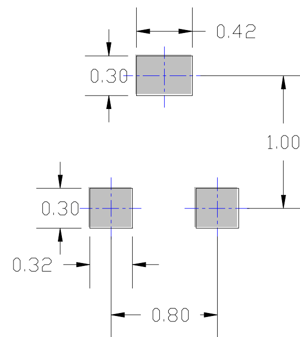
TOP VIEW



SIDE VIEW



SIDE VIEW



SUGGESTED SOLDER PAD LAYOUT

DIMENSIONS				
SYMBOL	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.017	0.022	0.430	0.550
A1	0.000	0.002	0.000	0.050
b	0.007	0.011	0.170	0.270
b1	0.011	0.015	0.270	0.370
c	0.003	0.008	0.080	0.200
D	0.045	0.049	1.150	1.250
E	0.045	0.049	1.150	1.250
E1	0.030	0.033	0.750	0.850
e	0.031TYP.		0.800TYP.	
θ	7°REF.		7°REF.	

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.