HC4812

40V Dual N-Channel MOSFET

General Description

These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

Features

V_{DS}	40V
I_D (at V_{GS}=10V)	18A
$R_{DS(ON)}$ (at V_{GS}=10V)	13mΩ(Max)

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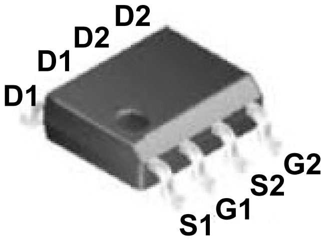

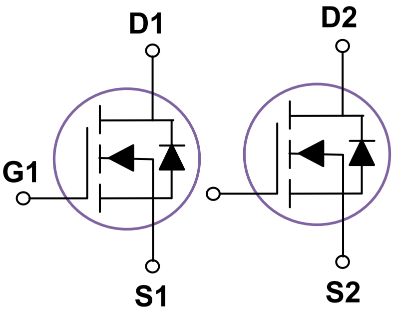

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±20	V
Drain Current-Continuous	TC=25°C	I_D	18	A
	TC=100°C	I_D	11	A
Drain Current – Pulsed		I_{DM}	72	A
Maximum Power Dissipation		P_D	2.1	W
Junction and Storage Temperature Range		T_J,T_{STG}	-55 To 150	℃

Thermal Characteristics

Parameter	Symbol	Typ	Max	Unit
Thermal Resistance junction-case	$R_{\theta Jc}$		1.1	℃ /W
Thermal Resistance junction-to-Ambient	$R_{\theta JA}$		60	℃ /W

Electrical Characteristics (TJ=25℃ unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V I_D=250μA	40			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=40V,V_{GS}=0V			1	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	1.2	1.8	2.5	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=10V, I_D=8A		10	13	mΩ
		V_{GS}=4.5V, I_D=4A		13	18	mΩ
gfs	Forward Transconductance	V_{DS}=10V , I_D=1A		5		S
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{DS}=25V,V_{GS}=0V, F=1.0MHz		1200		pF
C_{oss}	Output Capacitance			130		pF
C_{rss}	Reverse Transfer Capacitance			50		pF
SWITCHING PARAMETERS						
$t_{d(on)}$	Turn-on Delay Time	V_{DD}=15V,I_D=1A, V_{GS}=10V, R_G=3.3Ω		13		nS
t_r	Turn-on Rise Time			2.2		nS
$t_{d(off)}$	Turn-Off Delay Time			7.2		nS
t_f	Turn-Off Fall Time			4.5		nS
Q_g	Total Gate Charge	V_{DS}=20V,I_D=8A, V_{GS}=4.5V		12		nC
Q_{gs}	Gate-Source Charge			3.3		nC
Q_{gd}	Gate-Drain Charge			6.7		nC
V_{SD}	Diode Forward Voltage	V_{GS}=0V,I_{SD}=1A		0.72	1.4	V
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, F=1MHz		2.2		Ω

Note：

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%.
3. Essentially independent of operating temperature.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

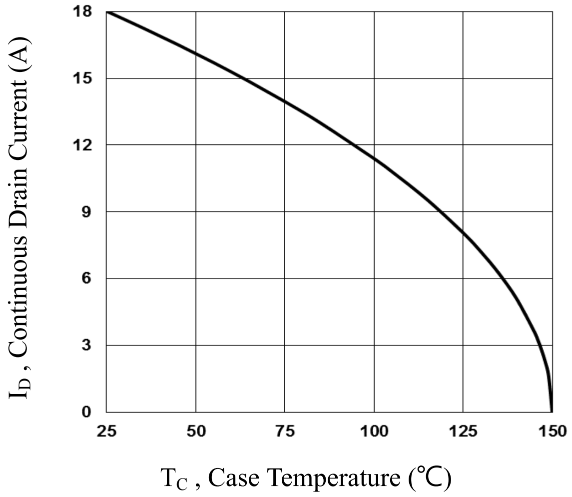

Fig.1 Continuous Drain Current vs. T_C

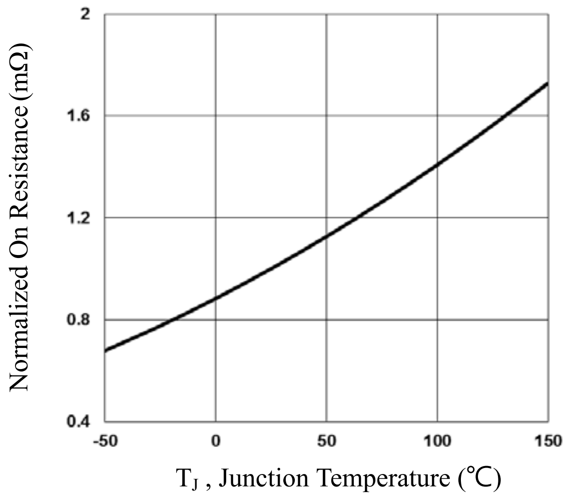

Fig.2 Normalized RDSON vs. T_J

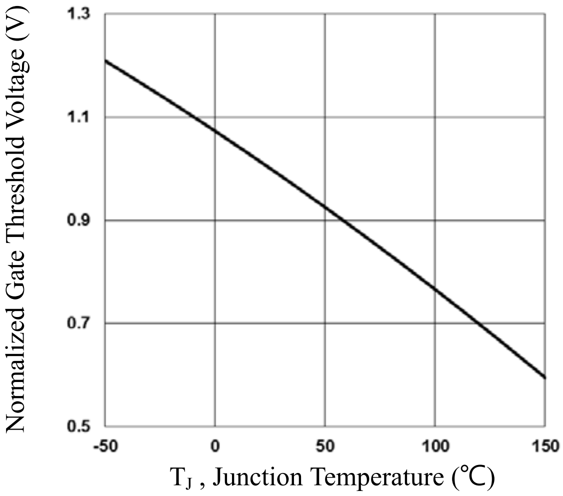

Fig.3 Normalized V_{th} vs. T_J

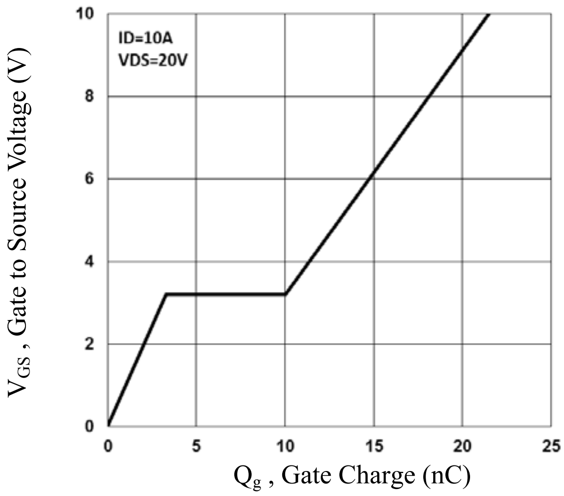

Fig.4 Gate Charge Waveform

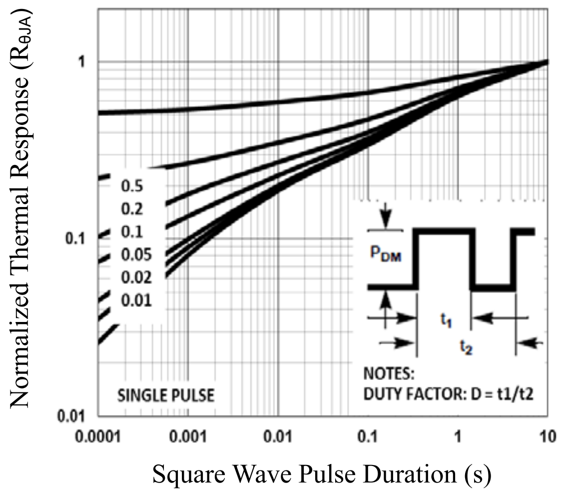

Fig.5 Normalized Transient Impedance

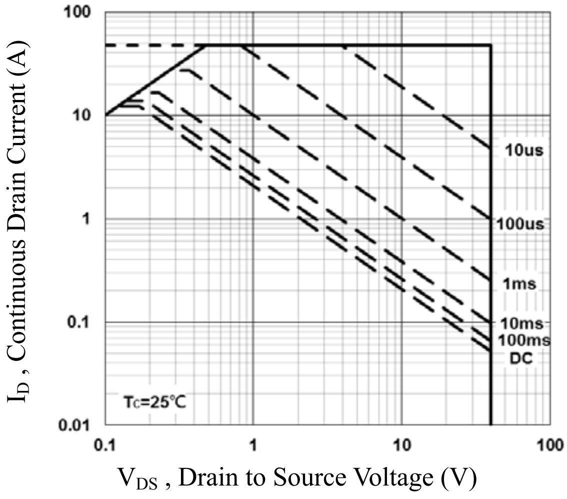

Fig.6 Maximum Safe Operation Area

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

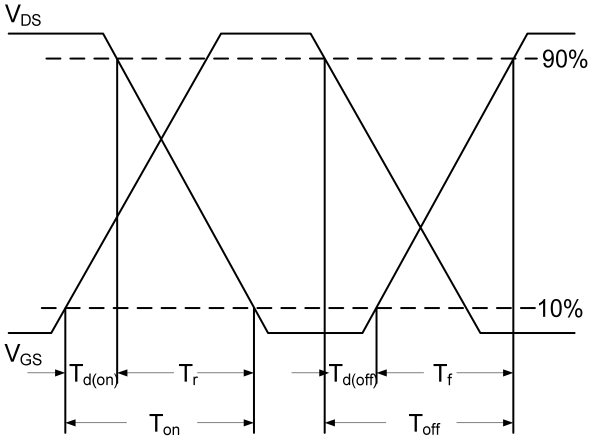

Fig.7 Switching Time Waveform

$$EAS=\frac{1}{2}L \times I_{AS}^2 \times \frac{BV_{DSS}}{BV_{DSS}-V_{DD}}$$

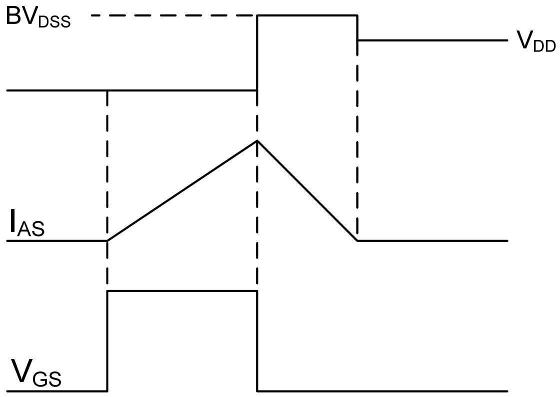

Fig.8 EAS Waveform

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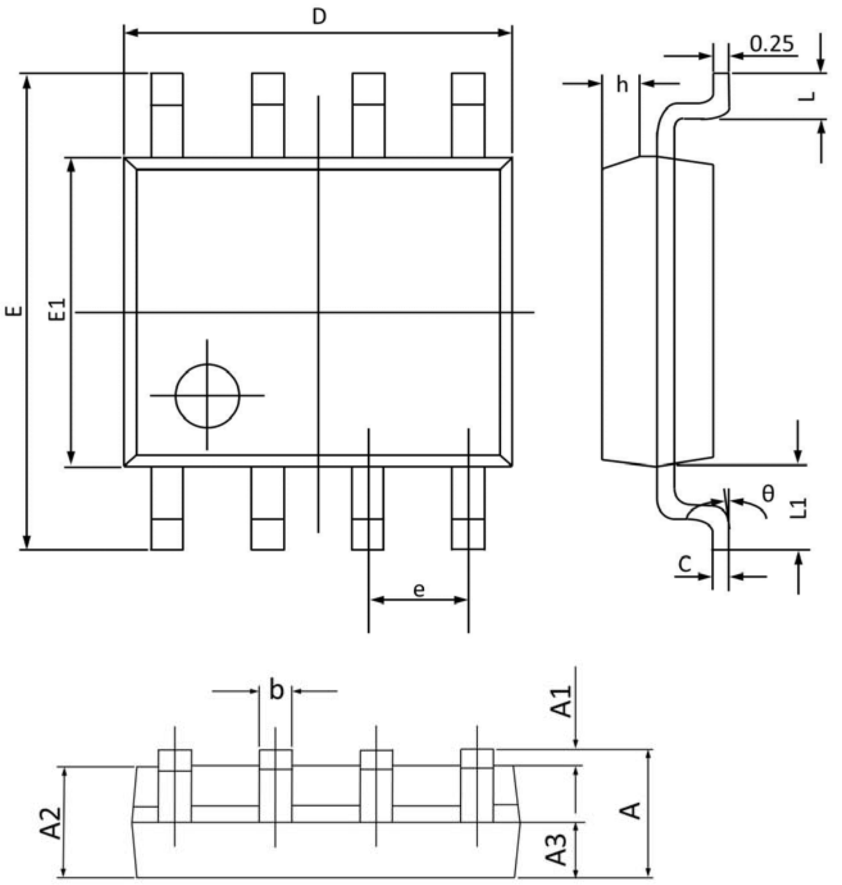

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.068
A1	0.100	0.250	0.004	0.009
A2	1.300	1.500	0.052	0.059
A3	0.600	0.700	0.024	0.027
b	0.390	0.480	0.016	0.018
c	0.210	0.260	0.009	0.010
D	4.700	5.100	0.186	0.200
E	5.800	6.200	0.229	0.244
E1	3.700	4.100	0.146	0.161
e	1.270(BSC)		0.050(BSC)	
h	0.250	0.500	0.010	0.019
L	0.500	0.800	0.019	0.031
L1	1.050(BSC)		0.041(BSC)	
θ	0°	8°	0°	8°