

HC4421

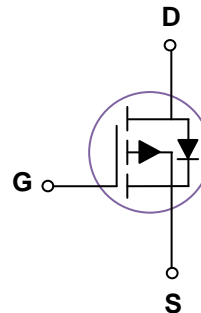
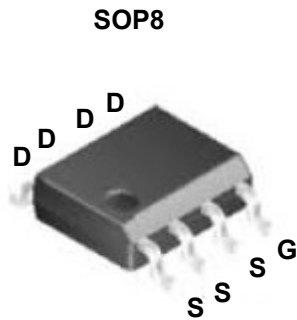
60V P-Channel MOSFET

General Description

These P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

Features

V_{DS}	-60V
I_D (at $V_{GS}=-10V$)	-6.0A
$R_{DS(ON)}$ (at $V_{GS}=-10V$)	50mΩ(Max)
$R_{DS(ON)}$ (at $V_{GS}=-4.5V$)	65mΩ(Max)



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units	
Drain-Source Voltage	V_{DS}	-60	V	
Gate-Source Voltage	V_{GS}	± 20	V	
Drain Current-Continuous	TC=25°C	I_D	-6.0	A
	TC=100°C	I_D	-4.2	A
Drain Current – Pulsed	I_{DM}	-25	A	
Maximum Power Dissipation	P_D	2	W	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	°C	

Thermal Characteristics

Parameter	Symbol	Typ	Max	Unit
Thermal Resistance junction-case	$R_{\theta Jc}$		1.1	°C /W
Thermal Resistance junction-to-Ambient	$R_{\theta JA}$		60	°C /W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250μA	-60			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-60V, V _{GS} =0V			1	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-1.0	-1.6	-2.2	V
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =-10V, I _D =-6.0A		42	50	mΩ
		V _{GS} =-4.5V, I _D =-5.0A		55	65	mΩ
DYNAMIC PARAMETERS						
C _{ISS}	Input Capacitance	V _{DS} =-30V, V _{GS} =0V, F=1.0MHz		2400		pF
C _{OSS}	Output Capacitance			175		pF
C _{RSS}	Reverse Transfer Capacitance			110		pF
SWITCHING PARAMETERS						
t _{d(on)}	Turn-on Delay Time	V _{DS} =-30V, I _D =-1A, V _{GS} =-10V, R _G =3Ω		9.8		nS
t _r	Turn-on Rise Time			6.0		nS
t _{d(off)}	Turn-Off Delay Time			44		nS
t _f	Turn-Off Fall Time			12		nS
Q _g	Total Gate Charge	V _{DS} =-30V, I _D =-5A, V _{GS} =-4.5V		22		nC
Q _{gs}	Gate-Source Charge			9.0		nC
Q _{gd}	Gate-Drain Charge			9.2		nC
V _{SD}	Diode Forward Voltage	V _{GS} =0V, I _{SD} =-1A		0.72	1.4	V

Note:

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
3. Essentially independent of operating temperature.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

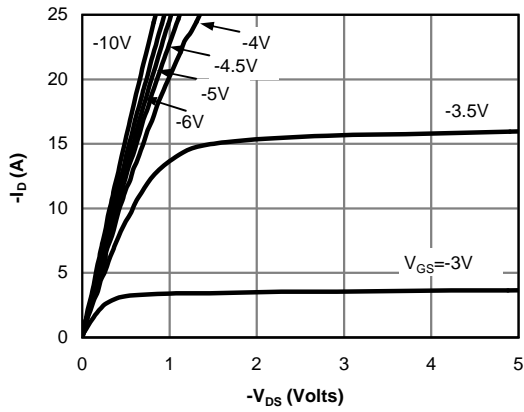


Figure 1: On-Region Characteristics

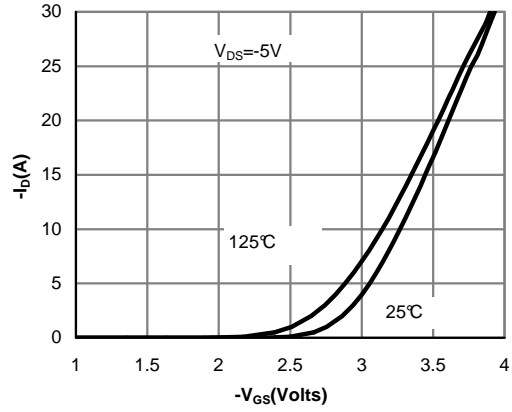


Figure 2: Transfer Characteristics

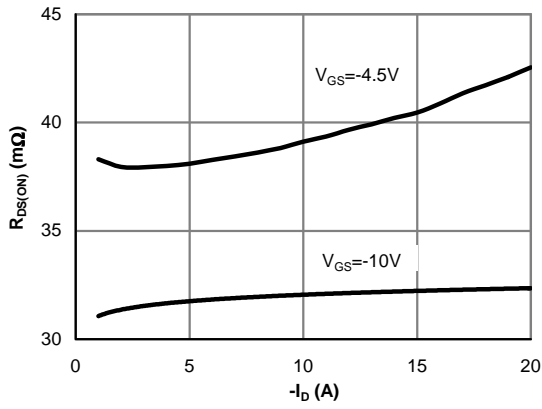


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

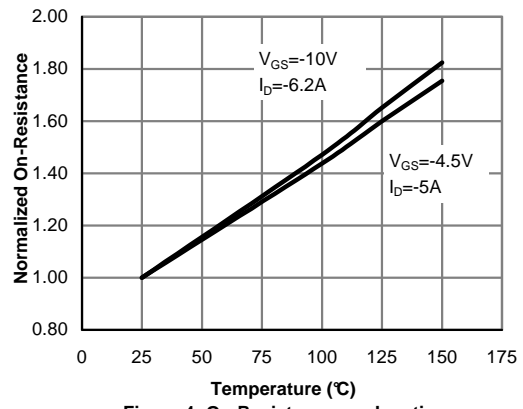


Figure 4: On-Resistance vs. Junction Temperature

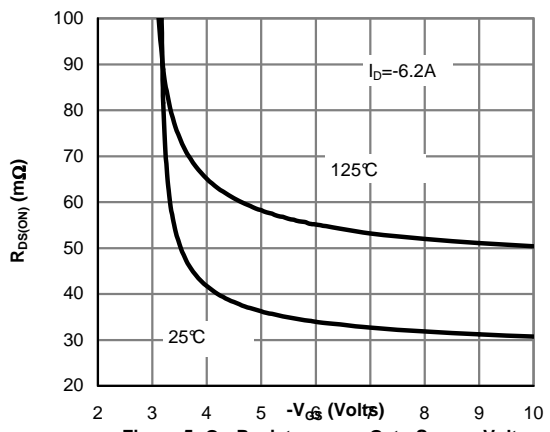


Figure 5: On-Resistance vs. Gate-Source Voltage

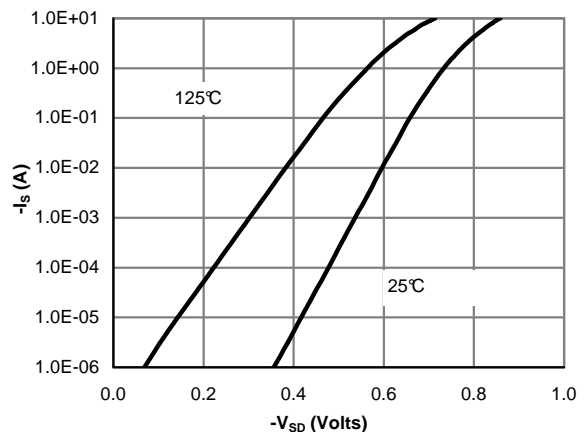


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

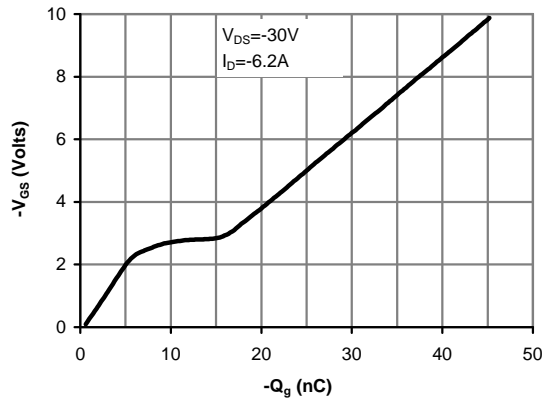


Figure 7: Gate-Charge Characteristics

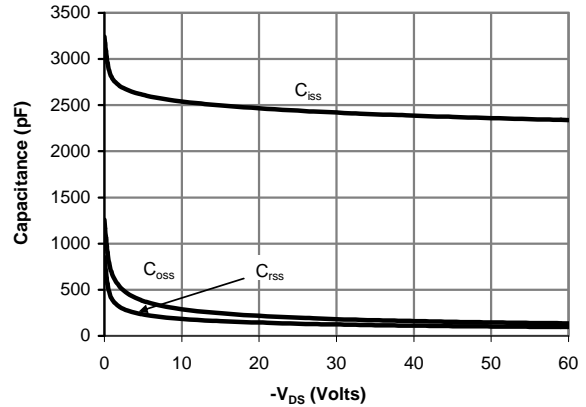


Figure 8: Capacitance Characteristics

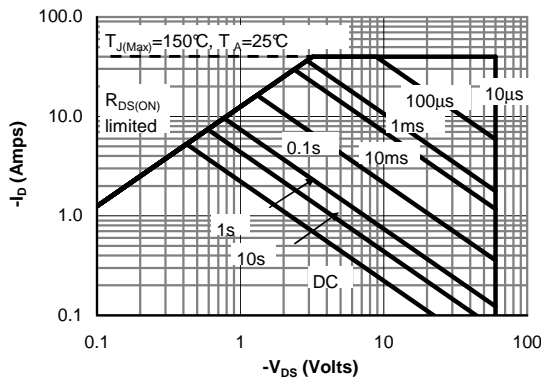


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

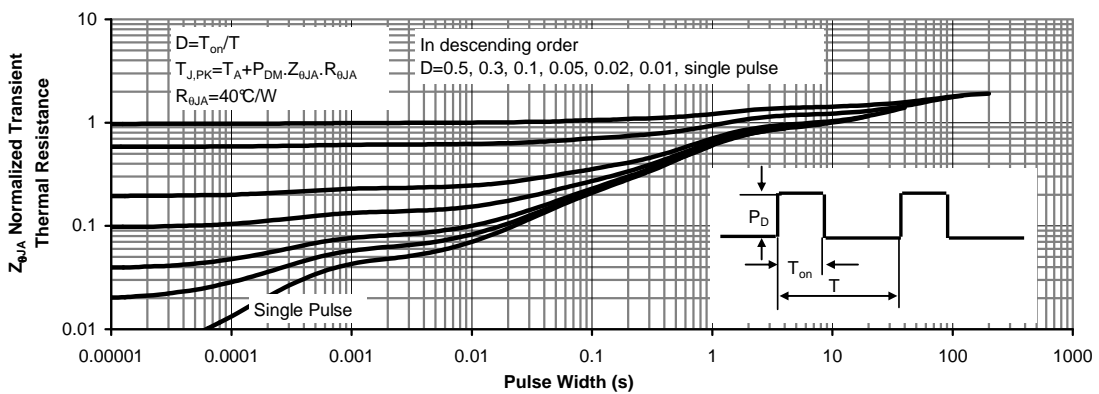
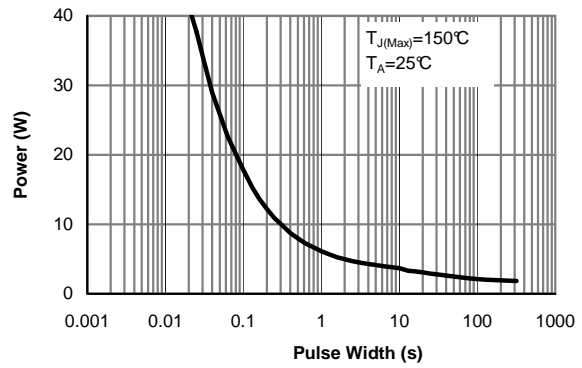
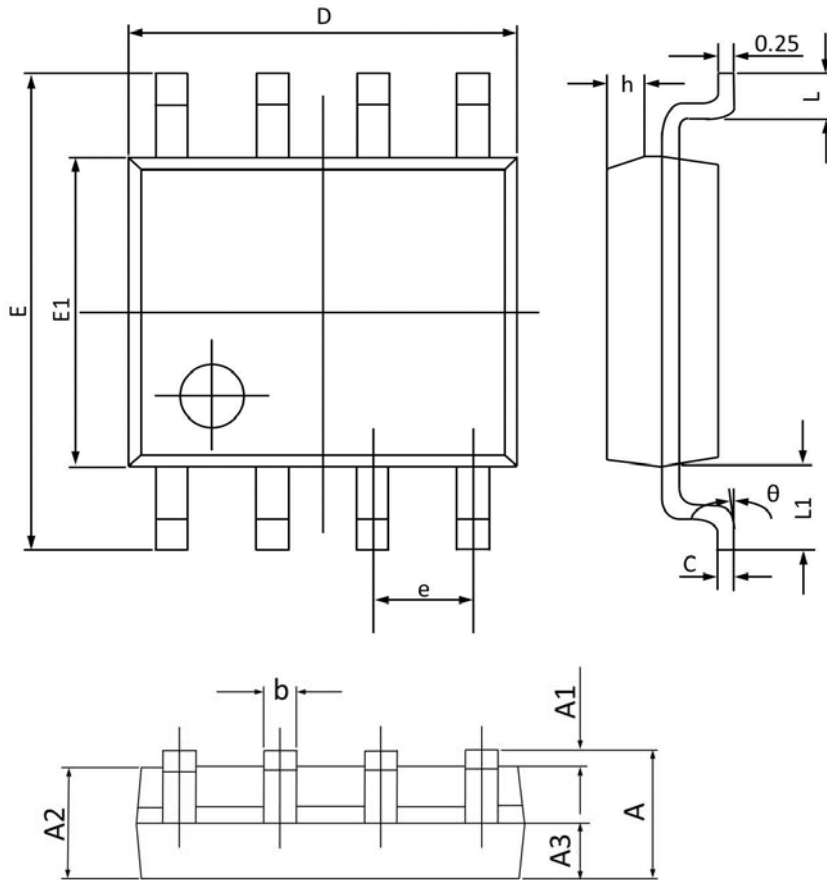


Figure 11: Normalized Maximum Transient Thermal Impedance

SOP8 PACKAGE INFORMATION



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.068
A1	0.100	0.250	0.004	0.009
A2	1.300	1.500	0.052	0.059
A3	0.600	0.700	0.024	0.027
b	0.390	0.480	0.016	0.018
c	0.210	0.260	0.009	0.010
D	4.700	5.100	0.186	0.200
E	5.800	6.200	0.229	0.244
E1	3.700	4.100	0.146	0.161
e	1.270(BSC)		0.050(BSC)	
h	0.250	0.500	0.010	0.019
L	0.500	0.800	0.019	0.031
L1	1.050(BSC)		0.041(BSC)	
theta	0°	8°	0°	8°