HC4614

40V N+P Dual Channel MOSFETs

General Description

These N+P dual Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

Features

V_{DS}	40V
I_D (at V_{GS}=10V)	8.0A
$R_{DS(ON)}$ (at V_{GS}=10V)	14mΩ(Typ)
V_{DS}	-40V
I_D (at V_{GS}=-10V)	-8.0A
$R_{DS(ON)}$ (at V_{GS}=-10V)	28mΩ(Typ)

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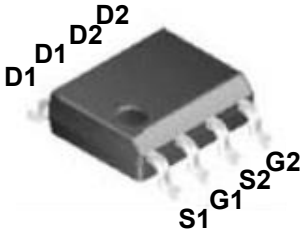
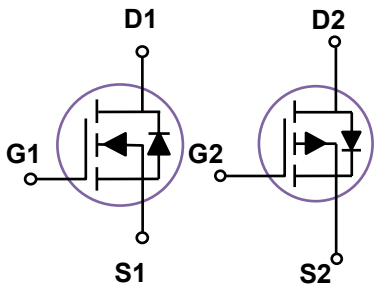




Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum		Units
Drain-Source Voltage		V_{DS}	40	-40	V
Gate-Source Voltage		V_{GS}	±20	±20	V
Drain Current-Continuous	TC=25°C	I_D	8.0	-8.0	A
	TC=70°C	I_D	6.4	-6.4	A
Drain Current – Pulsed		I_{DM}	32	-32	A
Maximum Power Dissipation		P_D	2.5		W
Junction and Storage Temperature Range		T_J,T_{STG}	-55 To 150		℃

Thermal Characteristics

Parameter	Symbol	Typ	Max	Unit
Thermal Resistance junction-to-Ambient	$R_{\theta JA}$		62	℃ /W

N-CH Electrical Characteristics (TJ=25℃ unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V I_D=250μA	40			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=40V,V_{GS}=0V			1	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	1.2	1.6	2.5	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=10V, I_D=5.0A		14	19	mΩ
		V_{GS}=4.5V, I_D=3.0A		21	29	mΩ
gfs	Forward Transconductance	V_{DS}=10V , I_D=1A		5		S
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{DS}=20V,V_{GS}=0V, F=1.0MHz		960		pF
C_{oss}	Output Capacitance			100		pF
C_{rss}	Reverse Transfer Capacitance			95		pF
SWITCHING PARAMETERS						
$t_{d(on)}$	Turn-on Delay Time	V_{GS}=4.5V V_{DS}=20V ID=6A		5.2		nS
t_r	Turn-on Rise Time			14.5		nS
$t_{d(off)}$	Turn-Off Delay Time			24		nS
t_f	Turn-Off Fall Time			12		nS
Q_g	Total Gate Charge	V_{DS}=20V,I_D=6A, V_{GS}=4.5V		23		nC
Q_{gs}	Gate-Source Charge			3.5		nC
Q_{gd}	Gate-Drain Charge			5.3		nC
V_{SD}	Diode Forward Voltage	V_{GS}=0V,I_{SD}=1A		0.70	1.3	V

Note：

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%.
3. Essentially independent of operating temperature.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

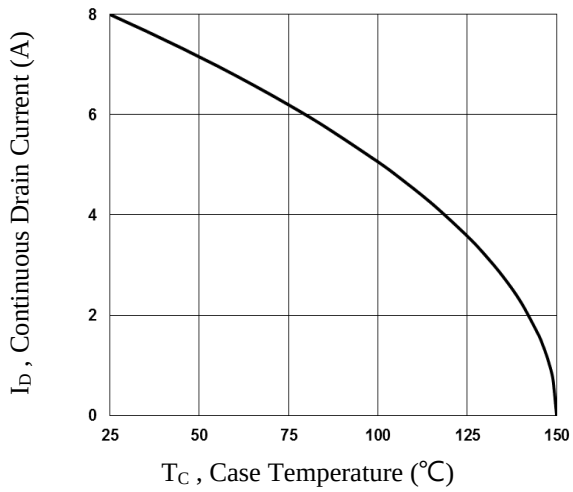


Fig.1 Continuous Drain Current vs. T_C

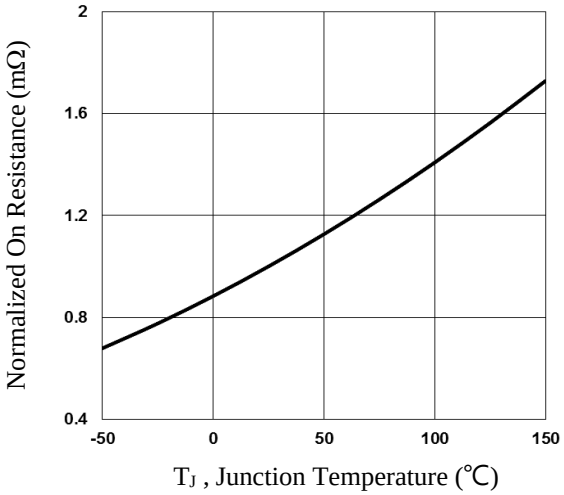


Fig.2 Normalized RDSON vs. T_J

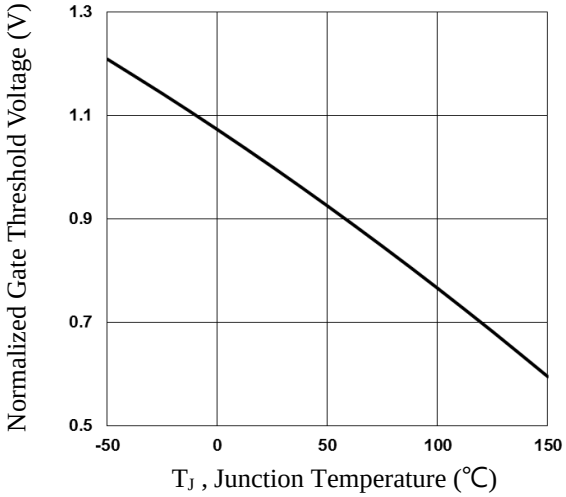


Fig.3 Normalized V_{th} vs. T_J

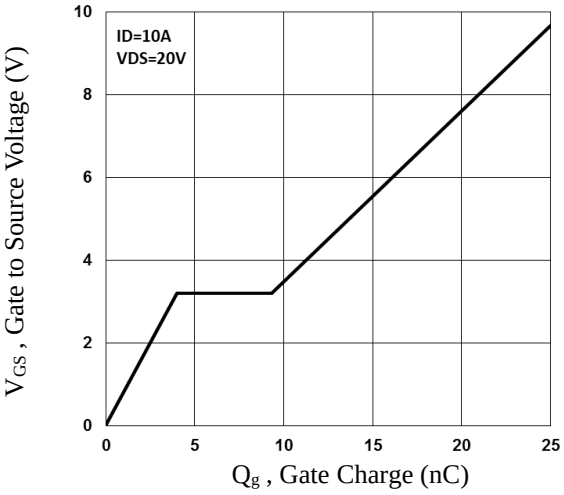


Fig.4 Gate Charge Waveform

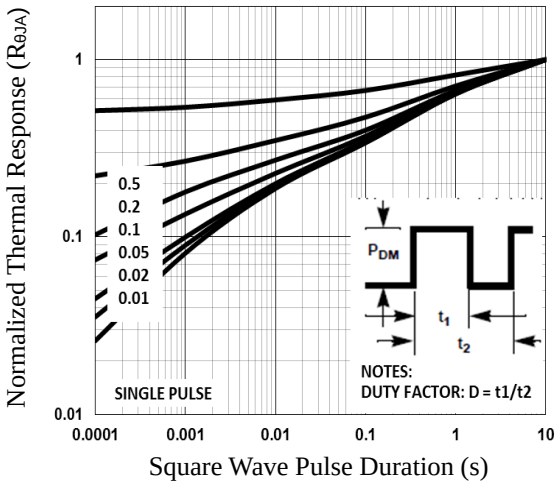


Fig.5 Normalized Transient Impedance

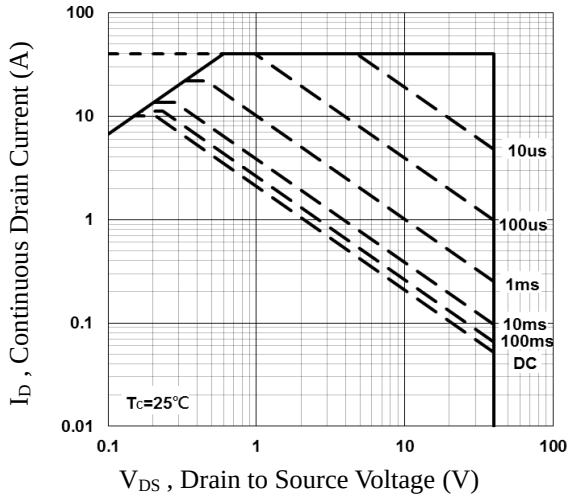


Fig.6 Maximum Safe Operation Area

P-CH Electrical Characteristics (TJ=25℃ unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V I_D=-250μA	-40			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-40V,V_{GS}=0V			1	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=-250μA	-1.2	-1.6	-2.5	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=-10V, I_D=-4.0A		28	35	mΩ
		V_{GS}=-4.5V, I_D=-2.0A		35	45	mΩ
gfs	Forward Transconductance	V_{DS}=-10V , I_D=-3A		6		S
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{DS}=-20V,V_{GS}=0V, F=1.0MHz		1320		pF
C_{oss}	Output Capacitance			116		pF
C_{rss}	Reverse Transfer Capacitance			89		pF
SWITCHING PARAMETERS						
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=-20V,I_D=-1A, V_{GS}=-4.5V, R_G=25Ω		12.8		nS
t_r	Turn-on Rise Time			8.7		nS
$t_{d(off)}$	Turn-Off Delay Time			65		nS
t_f	Turn-Off Fall Time			12.6		nS
Q_g	Total Gate Charge	V_{DS}=-20V,I_D=-10A, V_{GS}=-10V		23		nC
Q_{gs}	Gate-Source Charge			2.9		nC
Q_{gd}	Gate-Drain Charge			4.3		nC
V_{SD}	Diode Forward Voltage	V_{GS}=0V,I_{SD}=-1A		0.70	1.4	V

Note：

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%.
3. Essentially independent of operating temperature.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

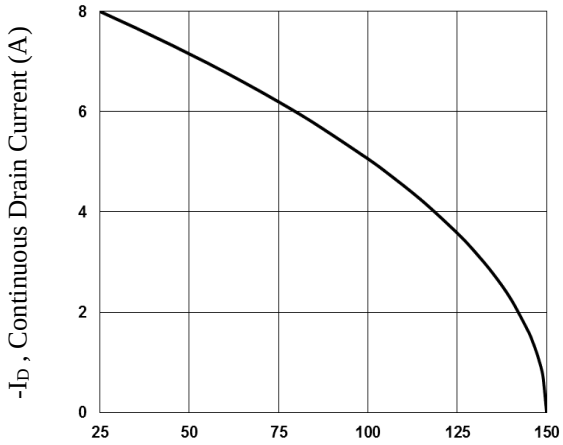


Fig.7 Continuous Drain Current vs. T_C

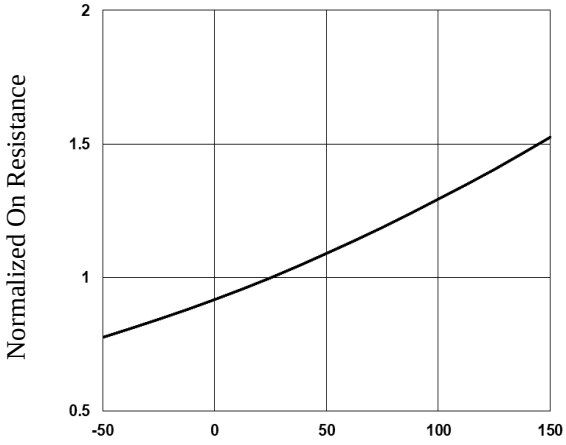


Fig.8 Normalized RDSON vs. T_J

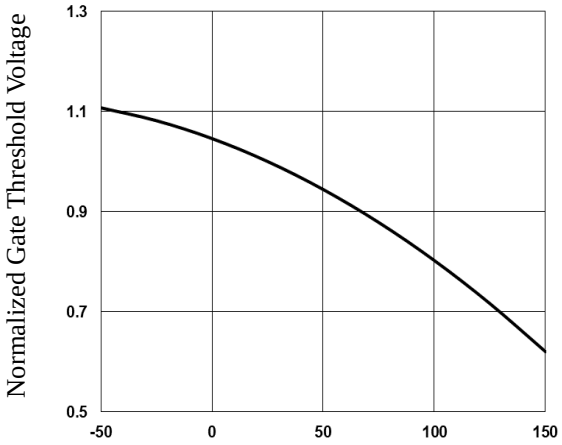


Fig.9 Normalized V_{th} vs. T_J

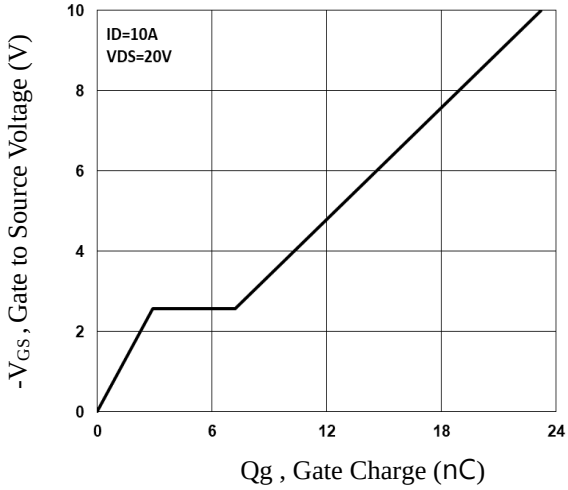


Fig.10 Gate Charge Waveform

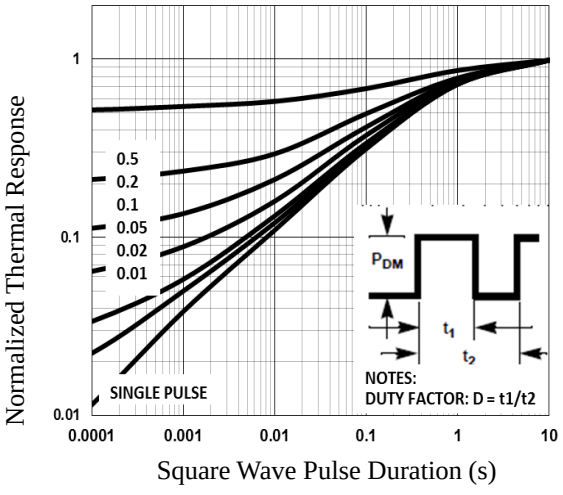


Fig.11 Normalized Transient Impedance

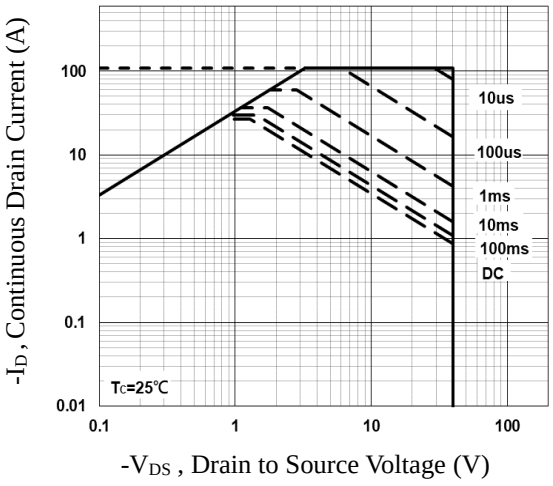
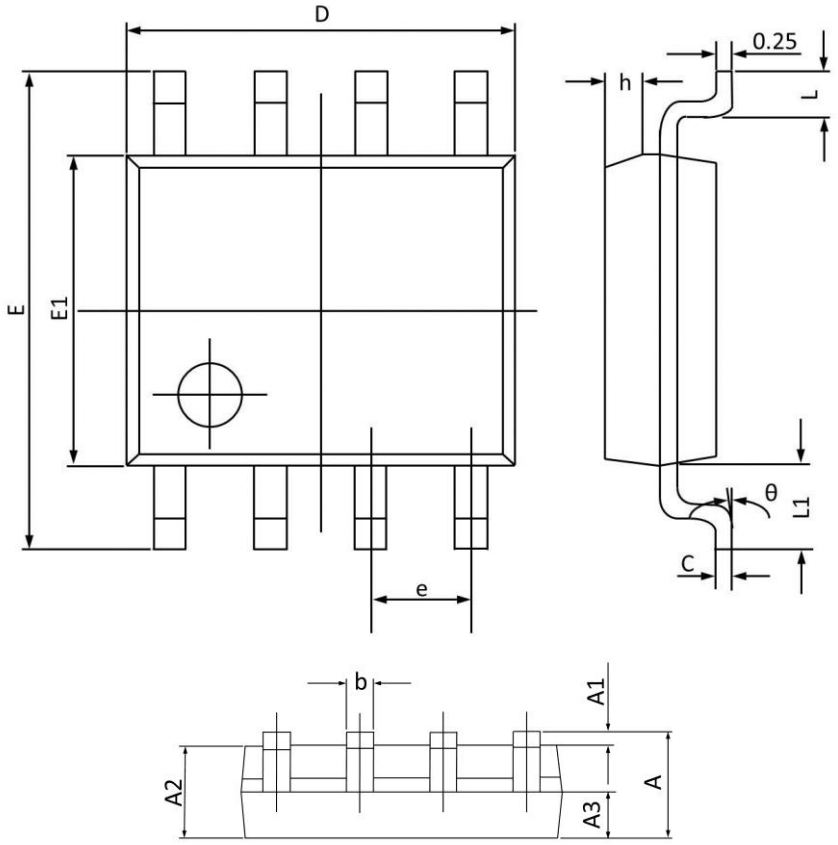


Fig.12 Maximum Safe Operation Area

SOP8 PACKAGE INFORMATION



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	1.650	0.049	0.065
A3	0.500	0.700	0.020	0.028
b	0.380	0.510	0.015	0.020
c	0.170	0.260	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.700	4.100	0.146	0.161
e	1.270(BSC)		0.050(BSC)	
h	0.250	0.500	0.010	0.020
L	0.400	0.800	0.016	0.031
L1	1.050(BSC)		0.041(BSC)	
θ	0°	8°	0°	8°